REMARKS

Claims 1-18 are pending in the application.

Section 103(a) Rejection:

The Office Action rejected claims 1 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Kim, et al. (U.S. Publication 2005/0125613) (hereinafter "Kim") and Beardsley, et al. (U.S. Patent 6,345,295) (hereinafter "Beardsley"), claims 2, 3, 11 and 12 as being unpatentable over Kim, Beardsley and Cherian, et al. (U.S. Patent 5,930,497) (hereinafter "Cherian"), claims 4-6 and 13-15 as being unpatentable over Kim, Beardsley, Cherian and Arsenault, et al. (U.S. Patent 6,578,128) (hereinafter "Arsenault") and claims 7-9 and 16-18 as being unpatentable over Kim, Beardsley and Hughes (U.S. Patent 6,973,543).

Applicant's claim 1 recites

> "A processor comprising:
>
> a trace generator configured to generate a plurality of traces each including one or more operations, wherein said one or more operations are decoded from one or more instructions, wherein each of said one or more operations is associated with a respective address;
>
> a trace cache memory coupled to said trace generator, wherein said trace cache memory includes a plurality of entries each configured to store one of said plurality of traces;
>
> wherein said trace generator is further configured to restrict each of said plurality of traces to include only operations having respective addresses that fall within one or more predetermined ranges of contiguous addresses." (Emphasis added)

The examiner asserts Kim teaches "a trace generator configured to generate a plurality of traces each including one or more operations, wherein said one or more operations are decoded from one or more instructions, wherein each of said one or more operations is associated with a respective address" and "a trace cache memory coupled to said trace generator, wherein said trace cache memory includes a plurality of entries each configured to store one of said plurality of traces," as recited in Applicant's claim 1.

The Examiner acknowledges Kim does not teach the remaining limitations of claim 1. However, the Examiner asserts Beardsley teaches the remaining limitations. Applicant respectfully disagrees with the Examiner's characterization of Beardsley and the Examiner's combining of the references.

More particularly, Beardsley is directed to "conducting traces of events in a computer system attachment network, and more particularly, to traces conducted involving events at a plurality of intelligent interface adapters."

The Examiner asserts Beardsley teaches the limitation at col. 4, lines 24-31. Applicant respectfully disagrees. Specifically, Beardsley teaches at col. 4, lines 4-31

> "Typically, the address information is in a range of addresses reserved for the memory of the particular device or its attachments, called "mailboxes". Specifically, devices on the bus or communication path may communicate with each other with mailboxes. The mailboxes are put into a data structure called a "post office". Each mailbox has a start address and a range, and an array of mailboxes is a "post office". Thus, the post office is a multiple times the size of a mailbox range. As the result, each device may have more than one set of address ranges, comprising more than one mailbox, for example, for the adapter and for the attached external I/O.
>
> The trace tool address filter 32 is arranged to recognize the addresses that map to these structures.
>
> The address filter 32 is arranged to detect the information for each event supplied by the bus snoop 18 and to select event information having selected addresses in the header. Thus, if 4 devices are coupled to the communication path 16, then the address ranges of the mailboxes for the 4 devices and/or their attachments may programmed into the address filter. The address filter 32 will look for those addresses of information on the

> communication path from the snoop 18 in order to select and conduct traces for information which addresses any of the 4 devices. Alternatively, the user may wish to examine less than all of the devices, or if a number of the devices have contiguous address ranges, the user may program the trace tool control 12 to operate the address filter 32 to select fewer address ranges." (Emphasis added)

Specifically, Beardsley is teaching a trace tool that traces events (i.e., the determination of the state of interfaces or devices during an event, such as sending or receiving data, can be helpful in determining the cause of an error in the communication process.) (*See* Beardsley col. 2, lines 12-15) (Emphasis added)

Further, Beardsley teaches at col. 5, lines 16-23

> "A trace entry consists of:
> 1) The address on the bus for the bus event;
> 2) The data of the bus event;
> 3) The amount of data in the trace entry (the data length count); and
> 4) The elapsed time since the previous trace entry.
> The resultant trace entry is then stored in the selected trace buffer 34." (Emphasis added)

Applicant fails to see how any of the above passages are relevant to Applicant's claim 1. The trace entries disclosed in Beardsley are not trace cache entries, nor do the entries in Beardsley mean the same thing as Applicant's trace cache entries.

The Examiner further asserts that Kim and Beardsley "are analogous art in that they are from the same field of endeavor, that is, a system and/or method of memory control." Applicant respectfully takes exception to the Examiner's assertions. Applicant asserts, not only do the recited passages of Beardsley not teach the limitation as recited in Applicant's claim 1, Applicant submits Beardsley **is not** in the same field of endeavor. Applicant submits Kim is in the filed of microprocessor cache memory systems and Beardsley is directed to tracing of events in a computer system. Accordingly, in addition to the cited art not teaching Applicant's limitations, Applicant submits there is no motivation to combine the art as the Examiner has suggested.

Cherian is directed to a method and means for emulating realistic access requests used in static or dynamic performance testing of a disk-based storage subsystem. The method and means are based on the fact that a test driver can substitute for an actual application if an executing process generates a pattern of accesses to disk subsystem addresses as a prescribed random walk function among a cluster of contiguous tracks associated with the process. (*See* Cherian Abstract).

Arsenault is directed to a system having a memory with a plurality of contiguous processor memory regions and a plurality of processors. Each one of such processors is associated with a corresponding one of the processor memory regions. Each one of such processors provides a plurality of sets of successive processor addresses. The addresses in each one of such sets have a successive series of used addresses and a successive series of reserve addresses. (*See* Arsenault Abstract)

Neither Cherian nor Arsenault were relied upon to teach the limitations recited I Applicant's claim 1, and Applicant submits neither Cherian nor Arsenault teach or suggest the limitations recited in Applicant's claim 1.

The Hughes patent cannot be used for rejections under 35 U.S.C. § 103 in regard to the present application. According to 35 U.S.C. § 103(c), art which qualifies as prior art only under § 102(e), (f) or (g) is not available for rejections under § 103 if that art and the subject matter of the application under examination were owned by or subject to an obligation of assignment to the same assignee at the time the invention was made. The Hughes patent qualifies as prior art only under § 102(e), (f) or (g) since it was not published or patented until after the filing date of the present application. Also, at the time the invention was made, the subject matter of present application and the Hughes patent were both owned by or subject to an obligation of assignment to the same assignee, Advanced Micro Devices, Inc., as evidenced by the assignment for the present application recorded in the PTO at reel/frame 014894/0113 and the assignment for the Hughes patent recorded in the PTO at reel/frame 012011/0132. Therefore, per 35 U.S.C.

§ 103(c), the Hughes patent cannot be used for rejections under 35 U.S.C. § 103 in regard to the present application. Thus, the rejections must be withdrawn.

Accordingly, Applicant submits claim 1, along with its dependent claims, patentably distinguishes over Kim in view of Beardsley, over Kim in view of Beardsley, in further view of Cherian, and over Kim in view of Beardsley, in further view of Arsenault, for the reasons given above.

Applicant's claim 10 recites features that are similar to the features recited in Applicant's claim 1. Thus, for at least the reasons given above in the discussion of claim 1, Applicant submits claim 10, along with its dependent claims, patentably distinguishes over Kim in view of Beardsley, over Kim in view of Beardsley, in further view of Cherian, and over Kim in view of Beardsley, in further view of Arsenault.

CONCLUSION

Applicant submits the application is in condition for allowance, and notice to that effect is respectfully requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above-referenced application from becoming abandoned, Applicant(s) hereby petition for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-90300/RCK.

Respectfully submitted,

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